METHOD OF ADDITIONAL INDUCTANCE SELECTION FOR FULL-BRIDGE BOOST CONVERTER

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Abstract

Design and simulation problems of high power full-bridge boost converter with 175…320 VDC supply voltage are considered. The converter under investigation consists of a full-bridge inverter, a boost high-frequency transformer, a diode rectifier connected to a capacitive filter and an active load. Additional inductance, connected in series with the transformers primary winding, is brought in the converters structure to achieve soft commutation of power switches and limitation of the current switched by them, in order to improve the reliability of the device and increase its efficiency of energy conversion. Selection of the additional inductance value is an important task, because too much of it could not allow to provide load power requirements, and too small of it could bring about defects of expensive power semiconductor elements. The choice of additional inductance is also complicated by the difficulty of measuring the transformer leakage inductance with sufficient accuracy. This problem is solved using the proposed method of selection the additional inductance value, based on an analysis of the mathematical model and on an analytical description of the output inverter current curve. The curves that measured on real device 60 kW (175 ... 320 V/ 610 V) show correctness of the model and the proposed method of selection the additional inductance value.

Key words

Full-bridge inverter, boost converter, soft commutation, phase-shift control, transformer leakage inductance.

1 Introduction

Power electronics development opens up prospects of energy converters design with high efficiency of semiconductor components usage and simultaneous improvement of weight-and-size indices of devices and cost reducing. But wide range of components, topologies and control schemes complicates the choice of an optimal topology of power cascade with reliable performance of the designed device. Simulation of impulse systems can solve this problem partly.

Scheme of full-bridge inverter with boost transformer is implemented for low input voltage and high output voltage and for high power converter. The advantage of it compared to buck-boost converter is galvanic isolation, and compared to half-bridge – half the value of switching current. But introduction of transformer complicates the converter analysis due to its non-ideality: it is rather difficult to estimate with sufficient accuracy the value of the transformer leakage inductance which brings significant changes to performance characteristics of the bridge inverter. At the same time, for the chosen topology “soft” commutation of the power switches could be ensured:

zero voltage switching (ZVS) mode of the power switches for full supply voltage range, and zero current switching (ZCS) for values closed to the minimum of supply voltage [Baei, Narimani, Moschopoulos, 2014].

This type of converters is implemented in various industries, such as oil plants, marine power systems and widely applied frequency converters with DC input voltage. There are different approaches to improving the scheme topology of ZVS full-bridge converters by additional components introduction such as auxiliary inductances, diodes, serially connected transformers [Koo, Moon, Youn, 2004; Jang, Jovanovic, 2004; Jain, Kang, Soin, Xi, 2002; Jang, Jovanovic, 2007; Jeon, Cho, 2001], but selection of these components and analysis of their characteristics requires time and increases the cost of the device.

In this paper we consider the full-bridge converter which topology consists of minimal quantity of elements and includes a full-bridge IGBT inverter, a boost transformer and a diode rectifier. The transformer leakage inductance value might not be enough for sot commutation mode ensuring and to limit the switching currents. In this case it is necessary to include additional inductance which can be connected both to primary and secondary transformer winding. Determination of the inductance value is a very important problem as its large values can lead to increasing of losses. Some researchers suggest determining its value from conditions based on unknown values: drain-to-source capacitance of MOSFET or collector-to-emitter capacitance of IGBT [Sabate, Vlatkovic, Ridel, Lee, Cho, 1990; Jeon, Cho, 2001].

There are also might be difficult to determine leakage inductance of real transformer windings as its value depends on frequency, core design, mutual position of primary and secondary windings and number of turns. There are many approaches to determine these values [Petrov, 1996; Hurley, Wilcox, 1994; Erickson, Maksimovic, 1998] - either experimental or theoretical investigations. Experimental approaches require taking into account ratio of measuring device accuracy and the measured value. Theoretical approaches require knowledge of design parameters values, but some of them might be unknown.

In this paper an approach for selection an additional inductance is proposed: its minimum value is obtained by modeling and simulation, and its maximum value is obtained by output inverter current curve analytical description.

The reminder of the paper is organized as follows. Section “Problem Statement” contains the converter functional diagram and its main characteristics. Also the problem of selection an additional inductance value is stated. A model and a simplified equivalent diagram of the investigated converter which allow analytical estimation of the minimum and maximum values of the additional inductance are received in section “Main Result”. Section “Example” contains data from the real device with power 60 kW (input 175-320 VDC; output 610 V/ 98 A) and numerical example which confirm correctness of the model and proposed method of selection the additional inductance value.

2 Problem Statement

Let us list the main parameters of the designed boost voltage converter: supply voltage is 175-310 V, rated supply voltage 250-280V, output stabilized voltage is 610 V. Maximum current switched by IGBT is 1250 A. Minimal output power is 60 W (current on the rectifier output not less than 100 A for 610 V). Parameters of the device power elements: transformer ratio is 1:6, capacitor bank capacity is 9900 μF, PWM carrier frequency is 7.5 kHz.

Converter considered in this paper consists of a full-bridge inverter loaded with power transformer which is connected to a rectifier [Chen, Lee, Jovanovic, Sabate, 1995]. Such a system should maintain predetermined average voltage (610 V) on the output of diode rectifier and filter by feedback control. Output voltage should be constant despite the changes of the input voltage. Selected structure of the converter includes transformer leakage inductance which value is impossible to be determined exactly. This fact complicates the choice of the additional inductivity.

Functional chart of the converter power part is shown in Fig.1. The following notations are used: DC – DC voltage source, VT1-VT4 – IGBT transistors of the full-bridge inverter, VD1-VD4 – diodes, L – additional inductivity, T – high frequency boost transformer, C_f – capacitive filter, R_l – active load resistance.

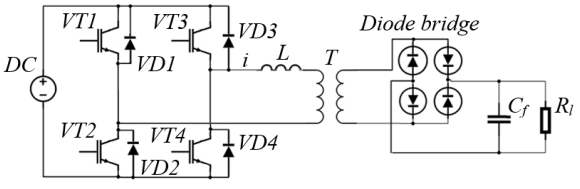

Figure 1. Functional chart of the converter

Let us state the problem of obtaining a computational model of the considered boost converter (see fig.1) and output inverter current curve analytical description to determine the minimum and

maximum values of additional inductance for the ensuring soft commutation mode and to limit switching current.

3 Main result

Consider model of the boost converter of 60 kW power with phase-shift switching algorithm of IGBT transistors.

The computational model of this system was created with Power Elements toolbox of Matlab Simulink and it is shown on fig.2. This model includes the subsystem "Bridge Inverter" shown in Fig 3.

In fig. 2 we use the following notations: L is inductor of the primary winding of the transformer, C_f is capacitive filter, R_l is active load resistance (chosen as 6.2 Ω which matches 60 kW); transformer is given as "Linear Transformer" element with rated power, frequency and voltages of primary and secondary windings. Resistance of the primary circuit is set very small, not equal to zero; its leakage inductance is 1 μH. Resistance R_m of the magnetizing circuit is set very large. Other windings parameters are set equal to zero. Value of the additional inductance is set approximately 3 μH.

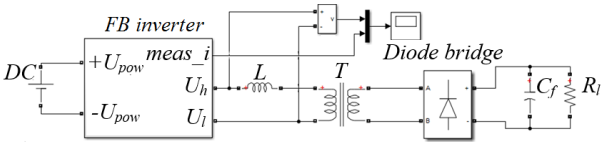

Figure 2. The computational model of the DC-DC converter.

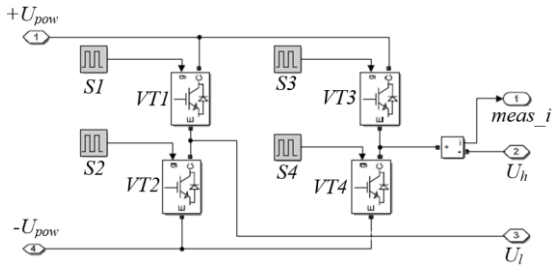

Figure 3. The subsystem "Bridge Inverter".

Fig. 4 shows multipolar rectangular pulses of the inverter output voltage with the same duration $0.5T_{PWM}K_{PWM}$ and amplitude 230 V equal to inverter supply voltage, where T_{PWM} is period of PWM carrier frequency, K_{PWM} is PWM coefficient. Fig.4 also shows control signals S1-S4 of the transistors VT1-VT4 respectively. It also shows there is a time delay between transistors control signals which ensures soft commutation of switches [Sabate, Vlatkovic, Ridel, Lee, Cho, 1990], switching at zero voltage. Control signals S3 and S4 are shifted with respect to S1 and S2 that is phase-shift control is realized and pre-assigned stabilized voltage on the converter output is obtained. Fig.5 shows current and voltage (between nodes 1 and 2 in fig.1) curves on the output of the full-bridge inverter (dashed and solid lines respectively).

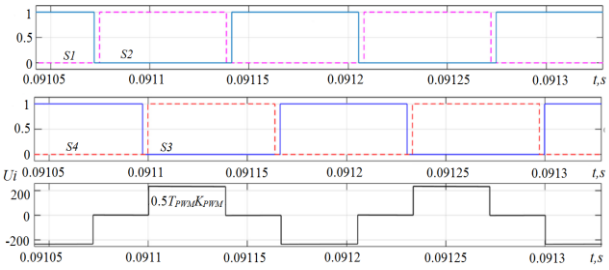

Figure 4. Control signals and output inverter voltage.

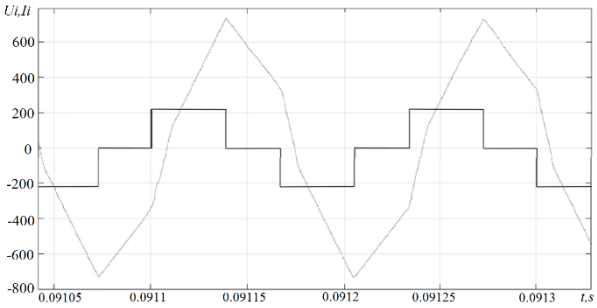

Figure 5. Output inverter current and voltage

Fig.5 illustrates the following transistors commutation law: transistors VT1, VT4 are switched on the first specific current plot area. Current from supply source flows through transistor VT1, inductance and the transformer primary winding (let us suppose that polarity is positive) then trough transistor VT4 to the supply source. Then VT1 is switched off and VT2 is switched on after time delay. During the time delay VD2 conducts current. After switching on of VT2 current flows through VD4 and VT2, the second specific current plot area appears and current may fall down to zero for small values of K_{PWM}. Then VT4 is switched off, VT3 is switched on after time delay, continuity of current in case it has not fallen to zero in ensured by diode VD3. Polarity of voltage of the inverter output is changed (VT2-VT3 are on). If current has not fallen to zero it is conducted by VD2-VD3, and it flows into supply source. Simultaneously negative polarity current grows in the load by VT2-VT3. Total current will fall down faster until it goes through zero, after that it growth (negative polarity) slows. If current falls to zero before the transistors switching, then negative polarity current growth will be observed after the switching thanks to pair VT2-VT3. Then transients repeat with negative polarity current.

The minimum value of the additional inductance is chosen by using the simulation: the maximum switched current value by the IGBT does not exceed a specified value with respect to given PWM carrier frequency, the maximum supply voltage and the minimum value K_{PWM}.

Consider the following substitution connection of the boost converter [Blache, Pierre, Cogitore, 1994].

In fig. 6 we use the following notations: L, R are inductance and resistance of the additional inductor; L_1, R_1 are leakage inductance and resistance of the primary transformer winding; L_m, L'_2, R'_2 are magnetizing, the secondary leakage inductance and winding resistance modified to the primary side; C_f, R_l are capacitance bank capacity and load resistance modified to the primary side.

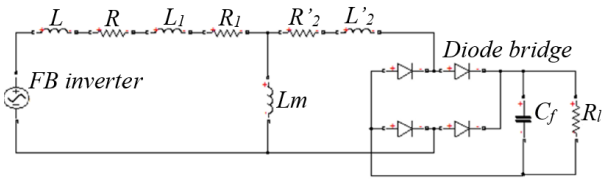

Figure 6. The equivalent circuit.

For influence analyses of the output filter capacity value on primary winding current we use simulations with filters of different capacities. Output current and voltage plots of the inverter are shown in fig.7 (I_{i1} corresponds to capacity of 9900 μF of capacitors bank, I_{i2} corresponds to capacity of 1100 μF).

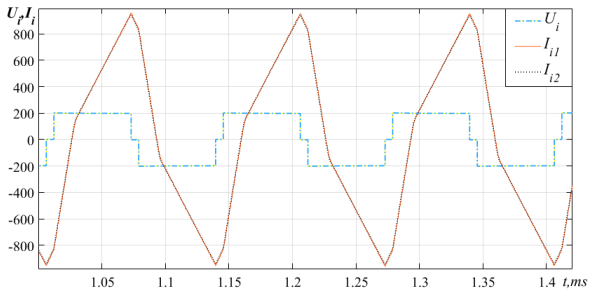

Figure 7. Output current and voltage plots of the inverter with different capacities.

Fig. 7 shows that current curves of primary winding capacity of 9900 μF and with capacity of 1100 μF of capacitors bank are nearly do not differ from each other. So we can conclude that due to high value of capacity a simplified substitution connection can be considered for qualitative and approximate quantitative description of the output inverter current as relation $(\omega C_f)^{-1} << R_l$ is correct. Fig. 8 shows simplified substitution connection where capacitor bank is substituted with ideal voltage source [Erickson, Maksimovic, 2001]. At short-circuiting of secondary winding through ideal voltage source relatively low current of transverse branch of the substitution transformer connection is not taken into account at calculations, so we can neglect magnetizing inductance. Then simplified substitution connection can be represented as RL circuit with parameters determined by parameters of transverse branch of the substitution connection shown in fig. 1.

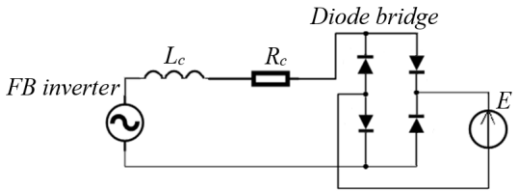

Figure 8. The simplified substitution connection.

Let us suppose that in fig.8 the inductance is $L_c = L + L_1 + L'_2$ and the resistance is $R_c = R + R_1 + R'_2$. Respect to the fact that RL time constant is greater than the carrier cycle, i.e. $L_c / R_c >> T_{PWM}$ ($R_C \approx 0$), exponent transient responses could be changed by linear processes [Charles, Sadiku, 2009], so when a positive voltage pulse appears at the inverter output, the output current will grow linearly according to the law:

$$i(t) = U_{sv}(t - t_d)/L_c. \qquad (1)$$

Due to fig. 5 and fig. 7 show steady-state processes, the beginning of positive current growth and the voltage jump are not synchronized and t_d is time delay (U_{sv} is supply voltage).

Then the current will go up until the end of the voltage pulse, the maximum value of it will be equal to:

$$I_{\max} = U_{sv}(T_{PWM} K_{PWM} - t_d)/L_c. \qquad (2)$$

At the end of the positive voltage pulse, the current will go down linearly according to the law, in which the reference time is beginning of zero-level of voltage:

$$i(t) = I_{\max}(1 - R_c t / L_c). \qquad (3)$$

After the occurrence of a negative voltage pulse, the rate of current decay increases:

$$i(t) = I_{\max}(1 - R_c t / L_c) - U_{sv}(t - t_p)/L_c, \quad (4)$$

where t_p is the time from reaching the maximum current to occurrence of the negative inverter output voltage.

It should be noted that in this section of the quasi-transient process a direction of an output inverter current does not coincide with the direction of the power source, i.e. the inverter supplies stored in the inductances energy to the power source. And the output inverter current lags behind the output inverter voltage.

The current will continue to go down until it becomes negative, the rectifier diodes will commutate, the polarity of the secondary winding voltage will change to the opposite, and the law of current variation will change to:

$$i(t) = U_{sv} t / L_c, \quad (5)$$

where time t is measured from zero-crossing of current. The further process is identical to that described above, only current values are negative.

The qualitative description of the inverter output current curve requires knowledge of the value of the total inductance. Accurate calculation of the inductance value is impeded by its dependence on many plant parameters, which are adjusted during the debugging of the device. However, when some of parameters of the converter, the transformer and the capacitor bank are fixed, estimation technique the maximum permissible value of the total inductance L_c could be really effective.

Estimation of the total inductance of the *RL* circuit can be obtained from (2):

$$L_c = U_{sv}(T_{PWM} K_{PWM} - t_d)/I_{\max}. \quad (6)$$

The maximum value L_C could be estimated from the fact that at pre-assigned values of T_{PWM}, minimum K_{PWM} and maximum supply voltage U_{sv} the transistor current should reach the possible maximum value, which is most often specified.

Fig. 9 (U_{sv} = 320 V, K_{PWM} = 0.17) shows that for low value of K_{PWM} time delay is approximately zero.

Then, according to the formula (6) and taking into account the fact that for a low value K_{PWM} $t_d = 0$:

$$L_c < U_{sv\_\max}(T_{PWM} K_{PWM})/I_{\max}. \quad (7)$$

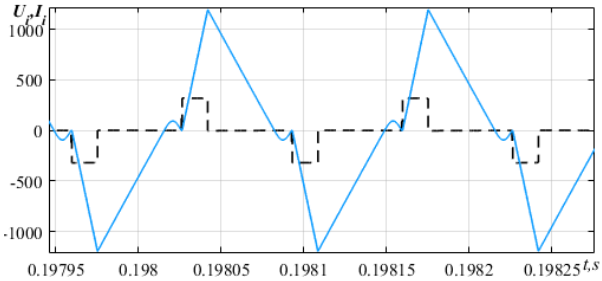

Figure 9. Output inverter current and voltage at U_{sv} = 320 V, K_{PWM} = 0.17.

Let us write down method of selection the additional inductance value.

Step 1. The minimum value of the additional inductance is chosen by using the simulation: the maximum switched current value by the IGBT does not exceed a specified value with respect to given PWM carrier frequency, the maximum supply voltage and the minimum value K_{PWM}.

Step 2. According to (7) find the necessary and sufficient value of the total inductance L_c.

Step 3. Calculate the transformer leakage inductance by using known techniques or from the (6) by using the experimental data without the additional inductance, estimate the value of the total inductance L_c approximately.

Step 4. Having received the values of the transformer leakage inductance and L_c, estimate the value of the additional inductance.

Step 5. In practice, it should be taken into account that K_{PWM} varies with voltage supply with regard to specified power roughly linearly. Therefore, the maximum total inductance should be set slightly less than the found one.

This technique is enough to specify parameters of the model. However, because of the difficulty of measuring the transformer leakage inductance with sufficient accuracy, the maximum value of the additional inductance should be selected based on the experimental data.

To study the prototype, an additional inductance should not be exceeding value $0.6L_c$.

4 Example

The leakage inductance transformer of the research prototype is known (it is conditioned by an elaboration of the transformer construction) and approximately equal to 1 μH. For specified characteristics $U_{sv\_\max} = 320$ V, $I_{\max\_z} = 1250$, $T_{PWM} = 1.33 \cdot 10^{-4}$ s the minimum value of additional inductance is defined from fig.9 ($I_{\max} = 1200$ A) and equal to

$L_{C\min} = 2.2$ μH by simulation. Due to K_{PWM} varies with voltage supply with regard to specified power linearly, i.e. K_{PWM} depends on relation $0.5U_{sv\_\min} / U_{sv\_\max}$ and for (7) it could be defined as $K_{PWM} \approx 0.28$ than $L_{C\max} = 9.26$ μH. With respect to step 5 the maximum value of additional inductance is $L_{\max} = 5.56$ μH.

The experimental data of 60 kW industrial prototype with specified characteristics and the additional inductance is about $L = 3$ μH are provided below in fig.10: (a) the full-bridge inverter output voltage (mirrored) and current (190 V/div and 600 A/div) U_{sv} = 187 V, $K_{PWM} = 0.35$ and (b,c) the full-bridge inverter output voltage and current for a low value K_{PWM} (190 V/div and 1200 A/div) U_{sv} = 320 V, $K_{PWM} = 0.18$. It is clear that simulated in fig.6 and in fig.9 and experimental in fig.10 results are similar.

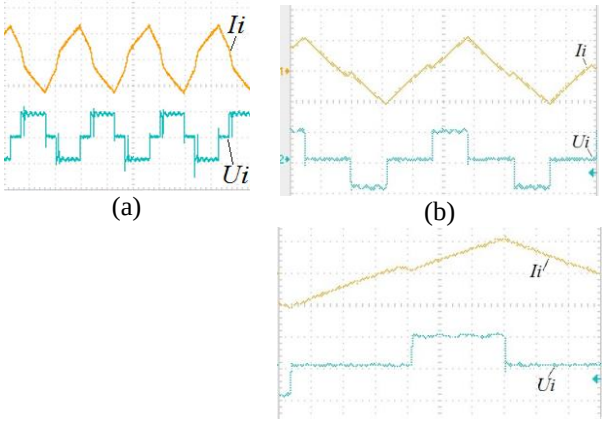

Figure 10. Experimental data.

Fig.10 illustrates that power switches work in the soft commutation mode, and it is possible to observe ZVS and ZCS at low value of K_{PWM}.

5 Conclusion

In this paper the high power full-bridge boost converter with a wide supply voltage range is considered. A new method of selection additional inductance value for achieving the soft commutation mode and for limitation current switched by IBGT based on simulation and analysis of the full-bridge inverter output current time curve is proposed. Analysis of the presented simulation data and experimental data of 60 kW industrial prototype (input 175-320 VDC; output 610 V/ 98 A) proves the validity of the proposed method.

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