DUFFING PHASE-LOCKED LOOP: EQUILIBRIUM AND PHASE JITTER

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Abstract

Since phase-locked loops (PLLs) were conceived by Bellescize in 1932, their presence has become almost mandatory in any telecommunication device or network, for being the essential element to recover frequency and phase information. Several models and implementation architectures appeared, following the strong electronic and computation evolution that occurs daily. As modeling and designing work together, considering the classical phase multiplier architecture, the nonlinearity is replaced by a polynomial approximation, making the differential equation describing the loop dynamics similar to the classical Düffing equation. As a result, the new model (Düffing PLL) presents a robust equilibrium performance and high immunity to accidental frequency modulation (phase-jitter), even for the first-order case, suggesting an interesting alternative implementation of PLLs.

Key words

Bifurcation, equilibrium, periodic perturbation, polynomial approximation, synchronization.

1 Introduction

Phase and frequency synchronization problems are present in electronic engineering since the first coherent modulation systems were developed, with the phase-locked loop implemented by using discrete components, performing the important function of detecting the time basis coming from a remote point [de Bellescize, 1932].

When the television systems were conceived, vertical and horizontal signals must had been synchronized by a periodic pulse, a function implemented by using the PLL architecture [Wendt and Fredendall, 1943]. For the development of color television, PLL were essential for synchronizing color beams [Richman, 1954].

Essentially, all of these PLL systems were a closed loop composed of a phase-detector (PD), a filter (F) and a voltage-controlled oscillator (VCO), as shown in Fig. 1. The PD compares the phase of the input signal, $v_i(t)$, coming from a remote point, with the phase of the local (VCO) oscillation, $v_o(t)$, producing an error signal that is filtered and controls the phase of the VCO signal.

Around 1965, the first PLL integrated circuits appeared, with all parts implemented with analogical components; however, with very low cost due to the wide range of their application [Best, 2007]. The digitalization of the PLL functions started in 1970 with the PD implemented by an exclusive or (X-OR) or charge pump circuit, presenting good performance [Gardner, 2005].

These developments were simultaneous with the digitalization of the telecommunication networks, in which all of the standard solutions are supposed to have synchronized time signals exchanged between the nodes [Bregni, 1998; Lindsey et. al, 1985].

With the development of the integrated services, the tendency to the digitalization of all network devices became mandatory, and the PLL, in spite of following the same Bellescize architecture, improved the manner of processing signals, originating the digital PLL (DPLL) circuits and converting the VCO function into digital [Bregni, 1998; Gardner, 2005; Meyr

and Ascheid, 1990].

As a consequence of the strong development of integrated circuits and digital filtering [Xiu et. al, 2004], the entire PLL started to be implemented by using flexible architectures, with adequate signal processing functions digitally implemented, generating the all-digital PLL (ADPLL) circuits, which is an important component of the new generation of wireless devices [Staszewski and Balsara, 2015].

Considering that this evolution allowed to have software implemented PLLs [Best, 2007], this work presents a new model for synchronizing signals based on the classical Bellescize's architecture [de Bellescize, 1932] of phase-locked loops. The idea starts by observing largely studied architectures [Best, 2007], with implementations present in almost all telecommunication networks or devices [Bregni, 1998; Leonov et. al, 2015], considering that a phase-detector compares the phases of two periodic signals, one coming from the exterior, with θ_i being the phase of $v_i(t)$, and another, from an internal oscillator, with θ_o being the phase of $v_o(t)$.

Defining phase error, $\phi = \theta_i - \theta_o$, the dynamics of these devices is described by:

$$L(\phi) - K \sin \phi = L(\theta_i), \tag{1}$$

with L being a linear operator and K representing the operational frequency band of the loop [Leonov et. al, 2015; Piqueira and Monteiro, 2006].

Inspired by an interesting work regarding economic temporal series [Kulkarni, 2013] and an exercise from a classical textbook [Guckemheimer and Holmes, 1983], a simple model for PLLs, which replaces the nonlinear term of equation (1) by a polynomial approximation is proposed:

$$\dot{\phi} = \dot{\theta}_i + \alpha\mu^2\phi + 2\mu\phi^3 - \phi^5, \tag{2}$$

with α representing the phase detection gain, and μ, with angular frequency dimension, representing the central frequency of the operational range of the PLL [Leonov et. all, 2015b].

Considering the similarity between equation (2) and Düffing equation [Guckemheimer and Holmes, 1983], the model proposed here will be called "Düffing PLL" (DF-PLL) and its main properties are discussed.

In the next section, the influence of parameters α and μ along with the bifurcations in the DF-PLL hold-in range [Leonov et. all, 2015b] are analyzed. The observed robustness of the equilibrium state guarantees that the zero or constant phase-error state is reachable, for any physical parameter combination.

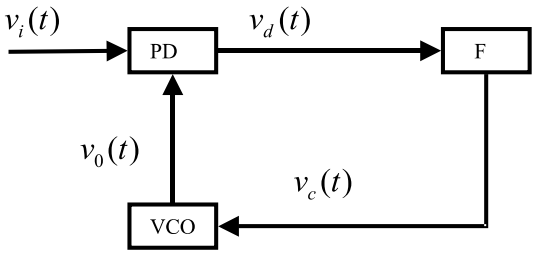

Figure 1. PLL block diagram

Following this reasoning, the phase-jitter phenomenon is modeled as a periodic perturbation of the equilibrium state, with frequencies about ten times higher than μ. Numerical simulations show that the DF-PLL rejects jitter in a very satisfactory manner. Lastly, some hints and conclusions are presented.

2 Bifurcation of the Equilibrium States

The DF-PLL hold in range is expressed by the equilibrium state of the dynamic equation (2), with $\dot{\theta}_i = 0$, i.e., when a phase step is applied to the input. Consequently, this equilibrium state corresponds to the roots of the polynomial: $\alpha\mu^2\phi + 2\mu\phi^3 - \phi^5$.

As real physical situations present positive values for the central frequencies of the operational range ($\mu > 0$), qualitative dynamical behavior of the equilibrium states depend only on a α that can assume any real value.

Starting with $\alpha < -1$, it can be seen that there is only one equilibrium state, $(\dot{\phi}, \phi) = (0, 0)$ which is asymptotically stable, as Fig. 2 shows for $\alpha = -2$ and $\mu = 2$. The asymptotically stability of the equilibrium state is derived from the calculation of the derivative of the vector field (2).

Increasing α, when it pass through $\alpha = -1$, the point $(\dot{\phi}, \phi) = (0, 0)$ remains asymptotically stable and two non-hyperbolic equilibrium points, $(\dot{\phi}, \phi) = (\sqrt{\mu}, 0)$ and $(\dot{\phi}, \phi) = (-\sqrt{\mu}, 0)$, appear, as Fig. 3 shows for $\mu = 2$.

For $-1 < \alpha < 0$, there are five equilibrium points: $(\dot{\phi}, \phi) = (0, 0)$, $(\dot{\phi}, \phi) = (\sqrt{\mu(1 + \sqrt{1+\alpha})}, 0)$ and $(\dot{\phi}, \phi) = (-\sqrt{\mu(1 + \sqrt{1+\alpha})}, 0)$, asymptotically stable; $(\dot{\phi}, \phi) = (\sqrt{\mu(1 + \sqrt{1-\alpha})}, 0)$, and $(\dot{\phi}, \phi) = (-\sqrt{\mu(1 + \sqrt{1-\alpha})}, 0)$, unstable, as Fig.

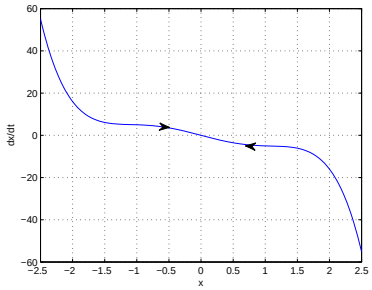

Figure 2. DF-PLL dynamical behavior of the equilibrium state for $\alpha = -2$

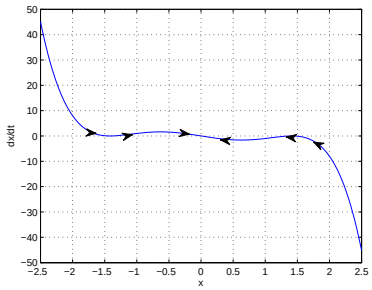

Figure 3. DF-PLL dynamical behavior of the equilibrium states for $\alpha = -1$

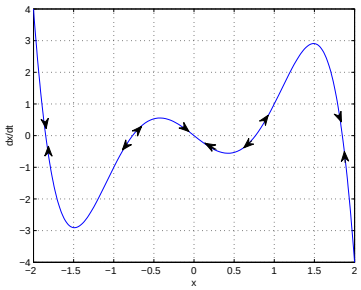

Figure 4. DF-PLL dynamical behavior of the equilibrium states for $\alpha = -0.5$

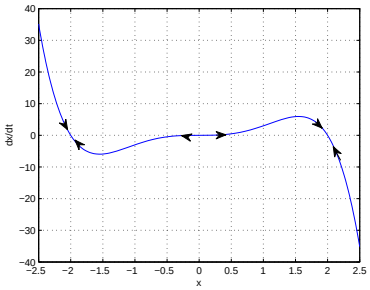

Figure 5. DF-PLL dynamical behavior of the equilibrium states for $\alpha = 0$

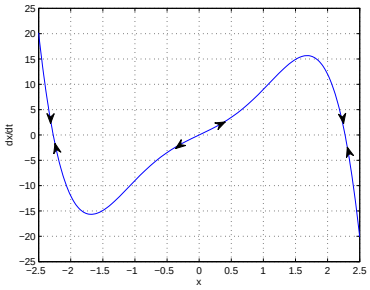

Figure 6. DF-PLL dynamical behavior of the equilibrium states for $\alpha = 1.50$

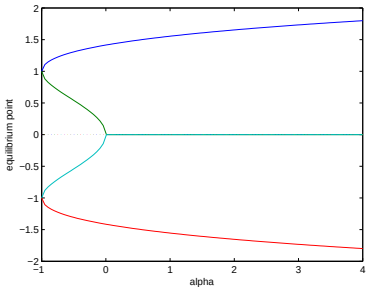

Figure 7. DF-PLL equilibrium state: bifurcation diagram

4 shows for $\mu = 2$.

When α pass through $\alpha = 0$, a new bifurcation occurs with $(\dot{\phi}, \phi) = (0, 0)$ becoming non-hyperbolic; $(\dot{\phi}, \phi) = (\sqrt{\mu(1+\sqrt{1+\alpha})}, 0)$ and $(\dot{\phi}, \phi) = (-\sqrt{\mu(1+\sqrt{1+\alpha})}, 0)$ remaining asymptotically stable; $(\dot{\phi}, \phi) = (\sqrt{\mu(1+\sqrt{1-\alpha})}, 0)$, and $(\dot{\phi}, \phi) = (-\sqrt{\mu(1+\sqrt{1-\alpha})}, 0)$ disappearing, as Fig. 5 shows for $\mu = 2$.

Considering $\alpha > 0$, $(\dot{\phi}, \phi) = (0, 0)$ becomes unstable; $(\dot{\phi}, \phi) = (\sqrt{\mu(1+\sqrt{1+\alpha})}, 0)$ and $(\dot{\phi}, \phi) = (-\sqrt{\mu(1+\sqrt{1+\alpha})}, 0)$ remain asymptotically stable, as Fig. 6 shows for $\mu = 2$.

The described results show the robustness of the locking process of DF-PLL, since the dynamic behavior of the phase error presents at least one asymptotically stable equilibrium state, for any value of α. Summarizing these points, Fig. 7 shows the bifurcation diagram related to the equilibrium states for the DF-PLL dynamics, considering $\mu = 1$.

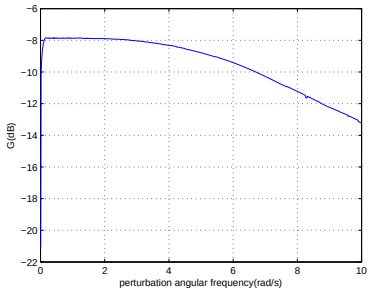

Figure 8. DF-PLL perturbation rejection

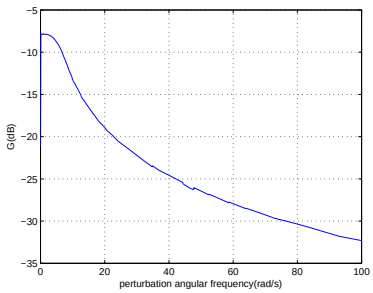

Figure 9. Jitter perturbation

3 Perturbation Rejection

For a precise time extraction strategy, the synchronization process provided by a PLL must reject phase variations originated by noise and imperfections of the transmission media, either long term (wander) or short (jitter) term ones [Meyr and Ascheid, 1990; Piqueira et. al, 2005; Piqueira and Caligares, 2006].

The evaluation of the DF-PLL perturbation was performed by using MATLAB-Simulink [Hanselman and Littlefield, 1996], starting with a zero phase error and considering the input phase, θ_i periodic with variable frequency. The parameters were adjusted for an asymptotically stable equilibrium situation with $\alpha = -1.5$ and $\mu = 2rad/s$.

The gain measure was defined by $G = 20log_{10}\frac{phaseerroramplitude}{perturbationamplitude}(dB)$ and the result is shown in Fig. 8. As it can be noticed, in the worst case, the phase error is $8dB$ attenuated related to the perturbation.

Besides, in the critical regions, wander ($\mu < 0.1rad/s$) and jitter ($\mu > 10rad/s$), the rejection increases drastically, as shown in Fig. 9 and 10, guaranteeing a good performance for the DF-PLL.

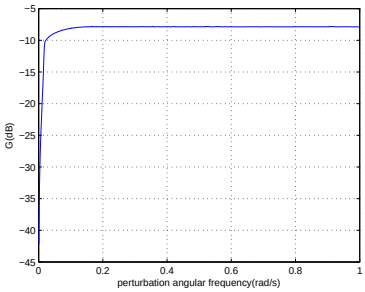

Figure 10. Wander perturbation

4 Final Hints

A new architecture (DF-PLL) was presented for the detection of time signals, based on the Düffing nonlinear equation. It was shown that DF-PLL presents a robust dynamics, concerning to equilibrium points.

Besides, DF-PLL presents a good performance when phase perturbations appear in the phase input, either in wander or in jitter case.

Conflict of interests

The authors declare that there is no conflict of interests regarding the publication of this article.

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