NONSMOOTH DYNAMICS AND FPIC CHAOS CONTROL IN A DC-DC ZAD-STRATEGY POWER CONVERTER

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Abstract

Nonsmooth phenomena such as discontinuity-induced bifurcations, due to saturations and switchings are reported in a power converter. They lead to chaos when a significant parameter is varied. Then, in this paper a novel tool for controlling chaos in a dynamical system is designed and applied to a buck converter driven with a PWM centered pulse and (Zero Average Dynamics) ZAD strategy. Chaotic operation has been stabilized with the so-called Fixed Point Induced Control (FPIC) technique. Numerical simulations and experimental results are reported. We can see in the results that the FPIC technique is a fast and efficient control for recovering stable periodic motion from chaotic operation. Appropriate software-reconfigurable hardware using a DSP-based rapid prototyping tool (RPT) is used to support the analytical and numerical discussion.

Key words

Piecewise-linear systems, Bifurcations, Chaos, DC-DC Converters, ZAD-strategy, FPIC technique.

1 Introduction

Switching sources are devices used in the implementation of power converters. One of its main drawbacks is the presence of chattering due to switching frequency, high order harmonic distortion and nonlinear phenomena. The latter can be dealt with control techniques (Poddar *et al.*, 1998), (Poddar *et al.*, 1995*a*), (Poddar *et al.*, 1995*b*), (Batlle *et al.*, 1999), (Batlle *et al.*, 1997), (Batlle *et al.*, 2000) while chattering and harmonic distortion are inherent to switching and can not be totally avoided. Fixed switching frequency improves performance even though chattering does not disappear. This is important in real applications, and to achieve this, some techniques have been developed: adaptive hysteresis band (Ruiz *et al.*, 1990), (Yao and Holmes, 1993), (Pinheiro *et al.*, 1994), signal injection with a selected frequency (Pinheiro *et al.*, 1994), (Silva and Snia, 1993), (Malesani *et al.*, 1996), (Nicolas *et al.*, 1996), zero average current in each iteration (ZACE) (Borle and Chemmangot, 1995) and recently zero average error dynamics in each iteration (ZAD).

ZAD control scheme, recently proposed in (Fossas *et al.*, 2001), tries to conjugate the advantages of fixed frequency implementations and the inherent robustness of sliding control modes. It is based on an appropriate design of the output that guarantees the fulfilment of the specifications and on a specific design of the Pulse Width Modulator duty cycle in such a way that the output average in each PWM-period is zero. A comparative study of this algorithm with respect to some of the previously reported in the literature can be found in (Biel *et al.*, 2002) and (Ramos *et al.*, 2003*a*).

The control action considered here, Zero Average Dynamics (ZAD) first proposed in (Fossas *et al.*, 2001), involves a direct design of the duty cycle and is implemented in a single, updated centered PWM (CPWM). For purposes of robustness, a linear combination of the error and its derivative is considered for the output as in (Bilalovic *et al.*, 1983), (Venkataramanan *et al.*, 1985), and (Carpita *et al.*, 1988). ZAD strategy and its application to power converters are extensively reported in (Fossas *et al.*, 2001), (Ramos *et al.*, 2003*b*), (Ramos *et al.*, 2002*b*), and (Ramos *et al.*, 2002*a*). The error dy-

namics time constant appears as a bifurcation parameter. As it varies, a very rich dynamics is observed in the controlled system. It has been reported in (Angulo *et al.*, 2005) that although the system is regulating in a wide region of the parameter space, the current waveform seems to be chaotic in a significant interval.

Thus, from a circuit design viewpoint, it is well worth determining which regions of the parameter space should be avoided. From a mathematical viewpoint, it is interesting to note which kind of bifurcations appear, especially if they are non-smooth and to determine the specific route to chaos. In this paper we are mainly due to the specific FPIC technique for controlling chaos. Details of the nonlinear phenomena in the ZAD-strategy controlled buck converter can be checked in (Angulo *et al.*, 2005).

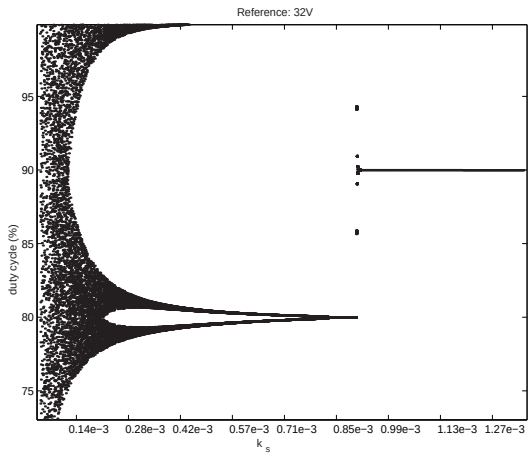

Figure 1. Bifurcation diagram of the duty cycle when a parameter (k_s) is varied.

The paper is structured as follows. After the introduction in Section 1, Section 2 describes the FPIC technique. Section 3 is devoted to the specific control technique when it is applied to a ZAD-strategy controlled buck converter. Section 4 describes the experimental setup and the results, and finally in Section 5 the conclusions can be found.

2 Fixed Point Induction Control (FPIC)

Let Σ be a discrete system

$$\mathbf{x}(k+1) = \mathbf{f}(\mathbf{x}(k), u(\mathbf{x}(k))) \tag{1}$$

where $\mathbf{x} \in \mathbb{R}^n$ and $\mathbf{f} : \mathbb{R}^{n+1} \mapsto \mathbb{R}^n$. Let $(\mathbf{x}^*, u^*)$ be a stable fixed point. Neither assumption is made on the stability of the controlled system, nor on the control law $u(\mathbf{x}(\cdot))$.

Result 1: Let $(\mathbf{x}^*, u^*)$ be a fixed point of $\mathbf{f}(\mathbf{x}, u)$ and assume that the eigenvalues of the linearised system at the fixed point have modulus less than 1, i.e.

$$|\lambda_i(\mathbf{J}_o)| := \left| \lambda_i \left(\left. \frac{\partial \mathbf{f}}{\partial \mathbf{x}} \right|_{(\mathbf{x}^*, u^*)} \right) \right| < 1 \ \ \forall i. \tag{2}$$

Then, the control input (FPIC technique)

$$\hat{u}(k) = \frac{u(\mathbf{x}(k)) + N u^*}{N+1} \tag{3}$$

stabilises the fixed point $(\mathbf{x}^*, u^*)$ for N sufficiently high.

Remark:
This situation is usual in bifurcations scenarios, where the stability of the equilibria is lost under the variation of parameters.

Proof:
The equation describing the system with the new controller is

$$\mathbf{x}(k+1) = \mathbf{f}(\mathbf{x}(k), \hat{u}(k)). \tag{4}$$

From Eq. (3) we have that $(\mathbf{x}^*, u^*)$ is still a fixed point of the discrete system (4). Linearising system (4) around the fixed point, we have

$$\mathbf{J}_n := \left. \frac{\partial \mathbf{f}}{\partial \mathbf{x}} \right|_{(\mathbf{x}^*, \hat{u}^*)} + \frac{\partial \mathbf{f}}{\partial \hat{u}} \frac{\partial \hat{u}}{\partial u} \frac{\partial u}{\partial \mathbf{x}} \tag{5}$$

that can be written as

$$\mathbf{J}_n = \mathbf{A}_1 + \mathbf{A}_2 \tag{6}$$

with $\mathbf{A}_1 = \left. \frac{\partial \mathbf{f}}{\partial \mathbf{x}} \right|_{(\mathbf{x}^*, \hat{u}^*)}$ and $\mathbf{A}_2 = \frac{\partial \mathbf{f}}{\partial \hat{u}} \frac{\partial \hat{u}}{\partial u} \frac{\partial u}{\partial \mathbf{x}}$, but

$$\mathbf{A}_2 = \frac{1}{N+1} \frac{\partial \mathbf{f}}{\partial \hat{u}} \frac{\partial u}{\partial \mathbf{x}},$$

and

$$\mathbf{J}_n = \mathbf{A}_1 + \frac{1}{N+1} \mathbf{A}_u \tag{7}$$

Now, using the theorem of continuity of the eigenvalues, we get that if N is sufficiently high, the eigenvalues of matrix $\mathbf{J}_n$ approximate the eigenvalues of matrix $\mathbf{J}_o$, and since all of them are inside the unit circle, system (4) is stable. $\triangleright$

3 Control of Chaos in a CPWM Buck Converter

This section starts describing the plant, a ZAD buck converter. Then, a Fixed Point Inductor Control (FPIC) scheme is used to stabilise 1-periodic orbits close to the chaotic attractor.

3.1 The buck converter

Fig. 2 shows a schematic diagram of a buck converter which can be modelled as the dynamical system

$$\begin{pmatrix} \dot{v} \\ \dot{i} \end{pmatrix} = \begin{pmatrix} -\frac{1}{RC} & \frac{1}{C} \\ -\frac{1}{L} & -\frac{r}{L} \end{pmatrix} \begin{pmatrix} v \\ i \end{pmatrix} + \begin{pmatrix} 0 \\ \frac{E}{L} \end{pmatrix} u \quad (8)$$

where r is the internal resistence of the inductor. Depending on the values of parameters R, L and C, the internal resistence r can be significant.

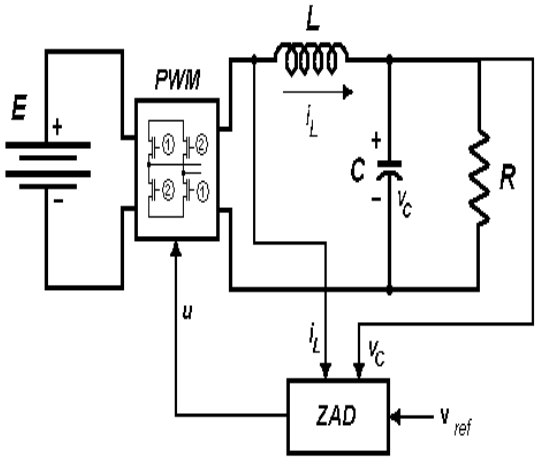

Figure 2. Scheme of the blocks diagram of a PWM ZAD-Strategy controlled buck DC/DC converter.

The capacitor voltage v and the inductor current i are the state variables. The control signal u takes discrete values $\{-1, 1\}$ depending on the switch position.

The system is controlled by PWM forcing zero average in the output $y = s(v, i)$ for each sampling period, i.e. $\forall k \geq 0$

$$\int_{kT}^{(k+1)T} s(v(t), i(t))dt = 0.$$

For robustness purposes output s, a proportional-derivative expression in the error, as in (Carpita *et al.*, 1988), is defined by

$$s(v, i) = (v - v_{ref}) + k_s(\dot{v} - \dot{v}_{ref}) \quad (9)$$

where v is the controlled variable, v_{ref} is the reference signal and k_s is the surface time constant. The control signal provided to the system is defined as follows

$$u = \begin{cases} 1 & \text{if } kT \leq t \leq k(1 + d/2)T \\ -1 & \text{if } k(1 + d/2)T < t < kT + (1 - d/2)T \\ 1 & \text{if } kT + (1 - d/2)T \leq t < (k + 1)T \end{cases} \quad (10)$$

where d is computed by

$$d = \left\{ \begin{array}{ll} 1 & \text{if } 1 \leq d_c \\ d_c & \text{if } 0 < d_c < 1 \\ 0 & \text{if } d_c \leq 0 \end{array} \right\} \quad (11)$$

Considering that $s(v, i)$ is approximately piecewise-linear, and after some algebraic manipulations, it can be shown that (Angulo *et al.*, 2005)

$$d_c = \frac{2s(kT) + T\dot{s}_2(kT)}{(\dot{s}_2(kT) - \dot{s}_1(kT))T}. \quad (12)$$

In Eq. (12) $s(kT)$ corresponds to the surface value when states are evaluated at $t = kT$. $\dot{s}_1(kT)$ is the surface slope with control signal $u = 1$ and $\dot{s}_2(kT)$ is the surface slope with $u = -1$. More details about this strategy can be found in (Fossas *et al.*, 2001). In what follows we will consider v_{ref} constant (and thus $\dot{v}_{ref} = 0$), which is the case for a regulation operation in the converter.

As it can be seen in Fig.1, as parameter k_s is reduced, a smooth period-doubling bifurcation is obtained. Then after a short range of parameter variation, one of the branches of the two-periodic stable orbit saturates due to a discontinuity-induced bifurcation. After another smooth period doubling bifurcation, leading to a four-periodic stable orbit another discontinuity-induced bifurcation occurs, where chaos appears (Angulo *et al.*, 2007).

3.2 FPIC Control of the CPWM Buck Converter

The duty cycle in the steady-state can be easily computed, and it is found to be

$$d_{ss} = \frac{1 + v_{ref}/E}{2}.$$

This allows applying the FPIC technique discussed in the previous Section. Now, the duty cycle to control the PWM is

$$d(k) = \frac{d + Nd_{ss}}{N + 1}$$

where d is defined in equation (11) and $N \geq 1$ for the parameter range used. Fig. 9 shows the results when the system is controlled in this way. We used in the experimental setup $E = 10$V, $v_{ref} = 8$V, $C = 690\mu$F, $L = 100\mu$H, $R = 30\Omega$, $r = 0.1\Omega$, and $T = 50\mu$s, and $N = 2$, operating in the chaotic zone. As it can be seen the unstable orbit achieves the stable 1-periodic. FPIC technique also allows stabilising higher periods orbits. As shown in 1 (Angulo *et al.*, 2005) when the stability of the 1-periodic orbit is lost, through a flip bifurcation, a stable 2-periodic orbit appears together with a 1-periodic unstable orbit.

4 Experimental setup

In this section we show with detail how an experimental setup can be built for checking the numerical results. Our experiments are based on a digital PWM. Digital-PWM has advantages such as: programmability, high flexibility, fewer components and advanced control algorithms.

4.1 Features of DSP

The DSP used is *DS1104 R&D Controller Board* of *dSPACE*. This system allows to develop digital controllers using the rapid control prototyping (RCP) tool. The real-time hardware based on a *PowerPC microprocessor* and its I/O interfaces make the board ideally suited for developing controllers in various fields: industry and university. Figure 3 shows a scheme of the basic architecture and I/O features of the DSP used.

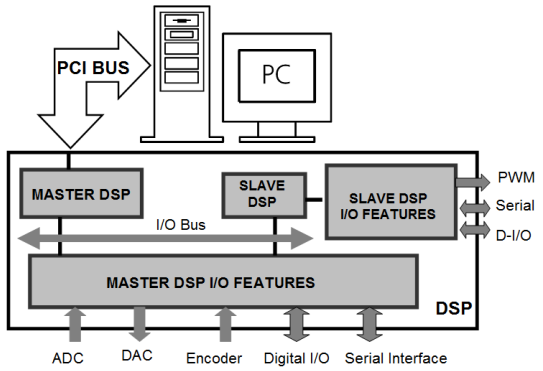

Figure 3. Scheme of the basic architecture and the functional units of the DSP.

The DSP can be plugged into a PCI slot of a PC. The DS1104 is specifically designed for the development of high-speed multivariable digital controllers and real-time simulations. The DSP system is based on a *603 PowerPC* floating-point processor running at 250 MHz. For advanced I/O purposes, the board includes a slave-DSP subsystem based on the *TMS320F240* DSP microcontroller. The *Master-DSP* includes: the PCI interface, the interruption controller, the memory comprising DRAM and flash memory and general-purpose timers. The Master-DSP I/O features are: ADC Unit with 4 channels of 16 bits and 4 channels of 12 bits; DAC Unit with 8 channels of 16 bits, the Bit I/O Unit, Incremental Encoder Interface and Serial Interface.

The Slave-DSP is a subsystem which consists of Texas Instruments TMS320F240 DSP running at 20 MHz. The slave DSP provides a timing I/O unit that can be used to generate and measure pulse-width modulated (PWM) and square-wave signals.

4.2 Digital-PWM Controllers

ZAD and FPIC controllers are designed in Simulink and then downloaded to a DSP, which provides the switching signals to the power electronics board. Figure 4 shows the basic scheme of hardware implementation of Digital-PWM controller of a power converter based on DSP.

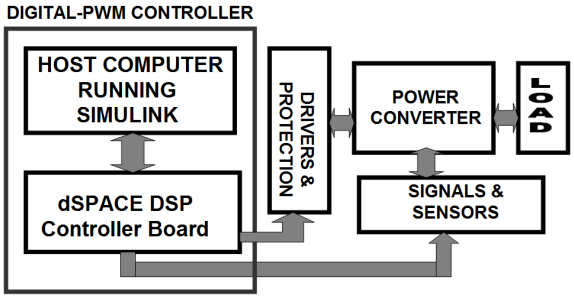

Figure 4. Hardware implementation of Digital-PWM controller of power converter based on DSP.

The high-level rapid prototyping tool of DSP has many advantages such as: the knowledge of coding in C or assembly language is not necessary; it is possible to use the same simulation blocks of Simulink in the hardware implementation; and the graphical interface which allows users real-time monitoring and parameter adjustments is easily used.

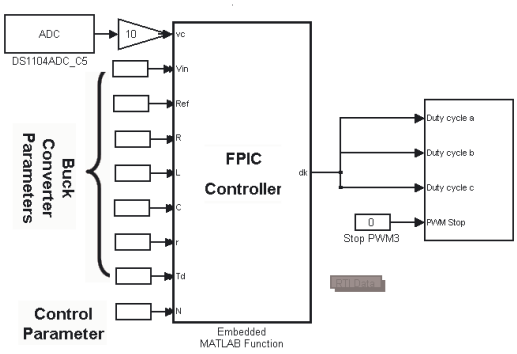

Figure 5. Simulink diagram of Digital-PWM FPIC controller.

ZAD and FPIC controllers designed for simulation are used for implementation. This block diagram is compiled and downloaded to the DSP and used for control of the buck converter. Figure 5 shows the Simulink diagram of Digital-PWM FPIC controller. In this example, only the capacitor voltage is sensed by the ADC channel. The FPIC algorithm is programmed in the Embedded Matlab Function and the duty cycle that it is sent to the buck converter by the PWM output of the slave DSP is and computed.

5 Bifurcation diagrams

In this section we show the experimental results, first, when no control action is done in the chaotic region, and only the ZAD strategy is active. Later, we activate the FPIC control to stabilize the chaotic region into a periodic orbit. The bifurcation diagram can be obtained on-line using *ControlDesk* software. This software communicates with *MATLAB-Simulink*, and it allows to acquire data and manage the controllers on the PC host.

5.1 ZAD Strategy without FPIC control

Fig.6 shows a numerically-computed bifurcation diagram of the voltage as we vary parameter k_s from 12 backwards. As it is shown, the converters operates quite well on a periodic orbit until $k_s \approx 1$. At this value, a bifurcation into chaotic motion is observed. Fig.7 shows the experimentally-computed bifurcation diagram, with good agreement.

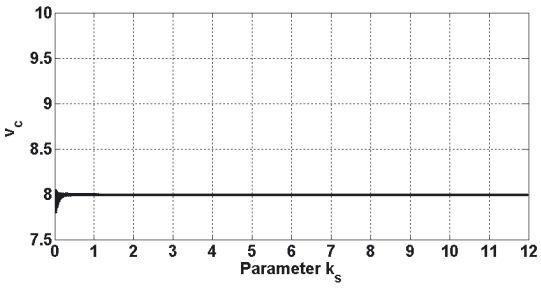

Figure 6. Numerically-computed bifurcation diagram for the ZAD-strategy control.

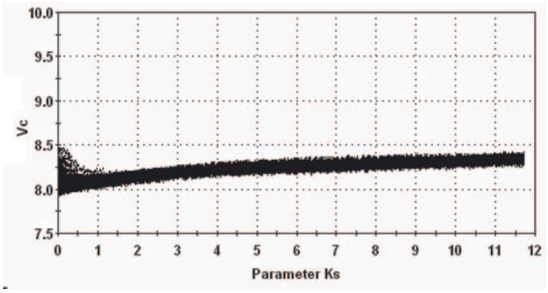

Figure 7. Experimental bifurcation diagram for the ZAD-strategy control.

5.2 ZAD Strategy with FPIC control

Now, we apply FPIC control (with $N = 2$) to enlarge the stability region. As it can be seen in Fig.8, the periodic orbit is stabilized in an additional range $[0.25, 1.00]$. Fig.8 shows a numerically-computed bifurcation diagram of the duty cycle while Fig.9 shows the experimentally-computed bifurcation diagram. A good qualitative agreement is shown. The differences are basically due to measurement issues.

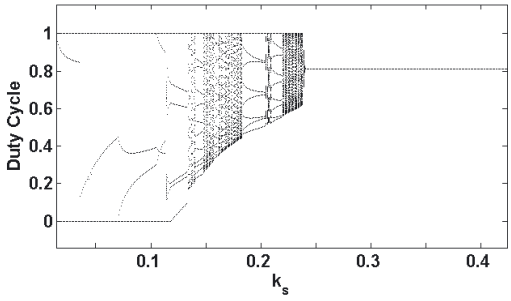

Figure 8. Numerically-computed bifurcation diagram for the ZAD-strategy control with FPIC.

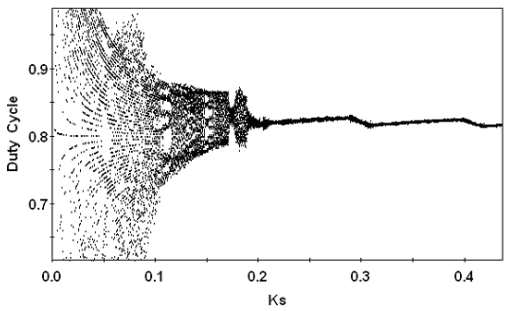

Figure 9. Experimental bifurcation diagram for the ZAD-strategy control with FPIC.

6 Conclusions

Numerical simulations and experiments show that the ZAD-strategy controlled buck converter develops several nonlinear and nonsmooth bifurcations as a parameter is varied. After a sequence of these bifurcations, chaos is obtained. In this paper we have shown the usefulness of a novel and simple stabilising technique for unstable and chaotic systems. Only analytical or numerical values of a steady-state control input guaranteeing a stable equilibrium point are needed. This

technique has been checked to be efficient for a CPWM with ZAD strategy, with very good results.

Simulations and laboratory experiments also show that the trade off the FPIC holds between the unstabilising control and a nominal control action, keeps the properties of the closed-loop controller.

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